EXHIBIT 1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; and MICRON TECHNOLOGY TEXAS LLC,
Petitioners,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2022-00418
U.S. Patent No. 8,301,833

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,301,833

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TABLE OF ABBREVIATIONS AND CONVENTIONS

Abbreviation	Meaning
'321 Application	U.S. Provisional Application No. 60/912,321
'586 Application	U.S. Provisional Application No. 60/941,586
'692 IPR	*SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00692, Paper 25 (PTAB July 5, 2018) (Final Written Decision)
'831 Patent	U.S. Patent No. 8,874,831
'833 Patent	U.S. Patent No. 8,301,833
'916 Application	U.S. Patent Application No. 12/240,916
Ashmore	U.S. Patent App. Pub. No. 2006/0212651
Best	U.S. Patent App. Pub. No. 2010/0110748 to Best
Bonella	U.S. Patent App. Pub. No. 2007/0136523 to Bonella
Dec.	Declaration of Ron Maltiel (Ex. 1003)
Long	U.S. Patent No. 7,421,552 to Long
Mills	U.S. Patent No. 6,026,465 to Mills

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I. Introduction

Petitioners request *inter partes* review ("IPR") of claims 1, 3-17, and 19-30 ("Challenged Claims") of U.S. Patent No. 8,301,833 ("'833 Patent").

The independent Challenged Claims (1 and 15) are unpatentable based on the effect of collateral estoppel. These claims are near identical, in relevant part, to claim 15 in related U.S. Patent No. 8,874,831 ("'831 Patent")—***which the PTAB previously invalidated as obvious*** in IPR2017-00692, Paper 25 (PTAB July 5, 2018). The present Petition asserts the same obviating prior art combination as in IPR2017-00692, and the Board should invalidate the claims here as it did in the prior well-reasoned opinion.

The remaining dependent Challenged Claims (3-14, 16-17, and 19-30), add nothing to the validity analysis, and are therefore unpatentable, as they merely recite well-known components and features that have been included in commonplace memory systems well prior to the '833 Patent's priority date.

II. Requirements for *Inter Partes* Review

This Petition complies with all statutory requirements, as well as 37 C.F.R. §§ 42.104, 42.105, and 42.15, and should be accorded a filing date pursuant to 37 C.F.R. § 42.106. The required fee is being paid electronically through PTAB E2E.

A. Certification

Pursuant to 37 C.F.R. § 42.104(a), Petitioners certify that the '833 Patent is available for IPR and Petitioners are not barred or estopped from requesting an IPR challenging the claims on the grounds identified herein.

B. Identification of Challenge

Under 37 C.F.R. §§ 42.104(b) and 42.22, Petitioners request that the Board institute this IPR on claims 1, 3-17, and 19-30 of the '833 Patent and cancel those claims as unpatentable for obviousness under pre-AIA 35 U.S.C. § 103 on the following grounds:

Ground	Claims	Basis for Unpatentability
1	1 and 15	Unpatentable as obvious under the doctrine of collateral estoppel
2	1, 3-17, and 19-30	Obvious over Best (Ex. 1006) in view of Bonella (Ex. 1008) and Mills (Ex. 1009)

III. The '833 Patent

A. Effective Filing Date

The '833 Patent resulted from Application No. 12/240,916 ("'916 Application"), filed September 29, 2008, a continuation of Application No. 12/131,873, filed on June 2, 2008 (abandoned). The '833 Patent claims priority to Provisional Application No. 60/941,586 ("'586 Application") (Ex. 1005), filed on June 1, 2007.

The Challenged Claims are **not** entitled to the benefit of the '586 Application's June 1, 2007 filing date because the '586 Application does not provide written description. 35 U.S.C. §§ 119(e), 112 (pre-AIA). Netlistcannot show[1] from the disclosure of the '586 Application that the inventors were in "possession" of the invention, i.e., that the written description "include[s] all of the limitations" of the claims or that "any absent text is necessarily comprehended in the description provided and would have been so understood at the time the patent application was filed." *Hyatt v. Boone*, 146 F.3d 1348, 1354-55 (Fed. Cir. 1998).

Netlist cannot make the requisite showing here. Specifically, claims 1 and 15, from which all the remaining Challenged Claims depend, recite at least the following features that lack written description support in the '586 Application[2]:

- "*the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency*."

[1] *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378-81 (Fed. Cir. 2015) (patent owner burden to show entitlement to provisional filing date).

[2] The features listed correspond to claim 15, but the corresponding features of claim 1 (which are not reproduced to avoid redundancy) also lack written description support in the '586 Application.

In fact, the '586 Application does not even include the words "clock" or "frequency," much less disclose anything remotely sufficient to show possession of volatile and non-volatile memory subsystems being operable at the clock frequencies recited in claims 1 and 15. *See* Dec., ¶¶ 55-56.

Further, the remaining Challenged claims all depend from either claim 1 or claim 15, and lack written description support in the '586 Application for the same reasons. The Challenged Claims are accordingly entitled to a priority date no earlier than **June 2, 2008**.[3]

B. Level of Ordinary Skill in the Art

As of June 2008 (or June 2007), a person of ordinary skill in the art ("POSITA") in the '833 Patent's field would have been a person with a bachelor's degree in materials science, electrical engineering, computer engineering, computer science, or in a related field and at least one year of experience with the design or development of semiconductor non-volatile memory circuitry or systems. *See* Dec., ¶¶ 48-52.

[3] As identified in §V.A.1-3, the references at issue herein are prior art even if the '833 Patent is entitled to claim priority to June 1, 2007.

C. Overview

The '833 Patent discloses a memory system that communicates with a host, such as a disk controller of a computer system. Ex. 1001, Abstract. The memory system can include volatile and non-volatile memory and a controller configured to backup the volatile memory using the non-volatile memory in the event of a trigger condition. *Id*. In order to power the system in the event of a power failure or reduction, the memory system can include a secondary power source such as a capacitor bank. *Id*. Figure 1 shows an example memory system:

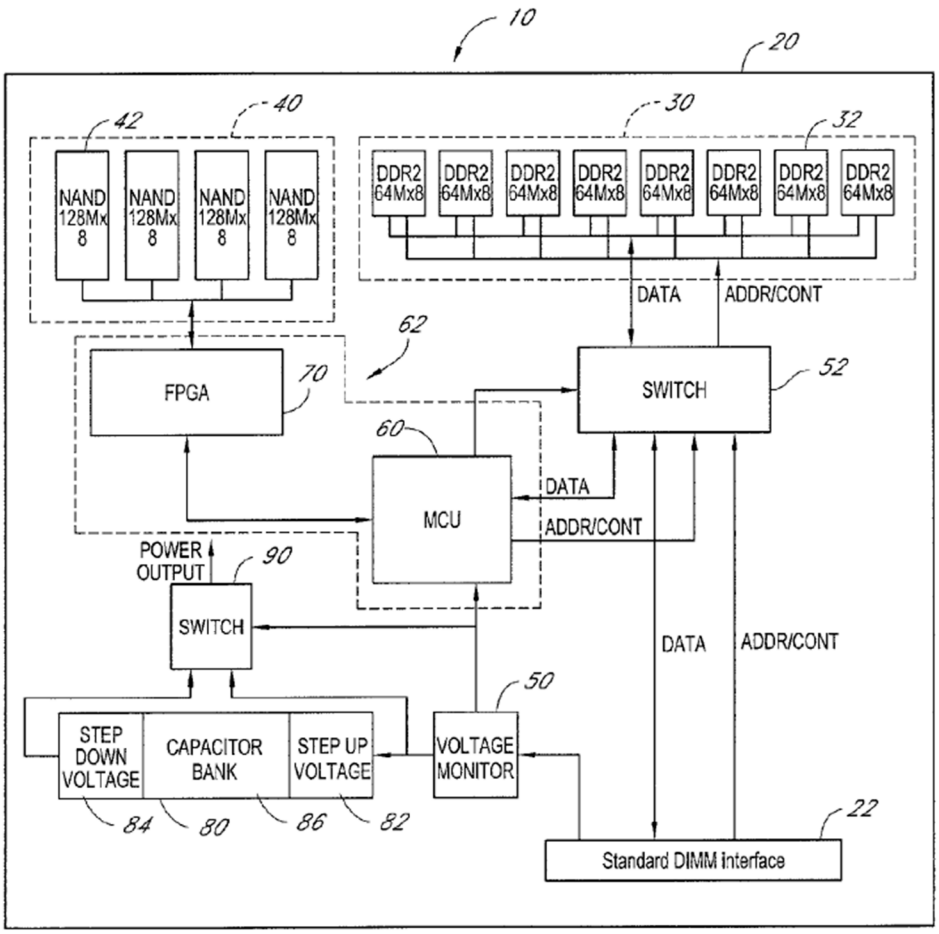


FIG. 1

Id., Fig. 1, 3:16-17; Dec., ¶¶ 57-58.

The volatile memory system can be operated at a reduced frequency during backup and/or restore operations to improve efficiency of the system and save power. Ex. 1001, 4:41-44. Figure 9 depicts an example method of operating a volatile memory subsystem at a reduced rate in a backup mode:

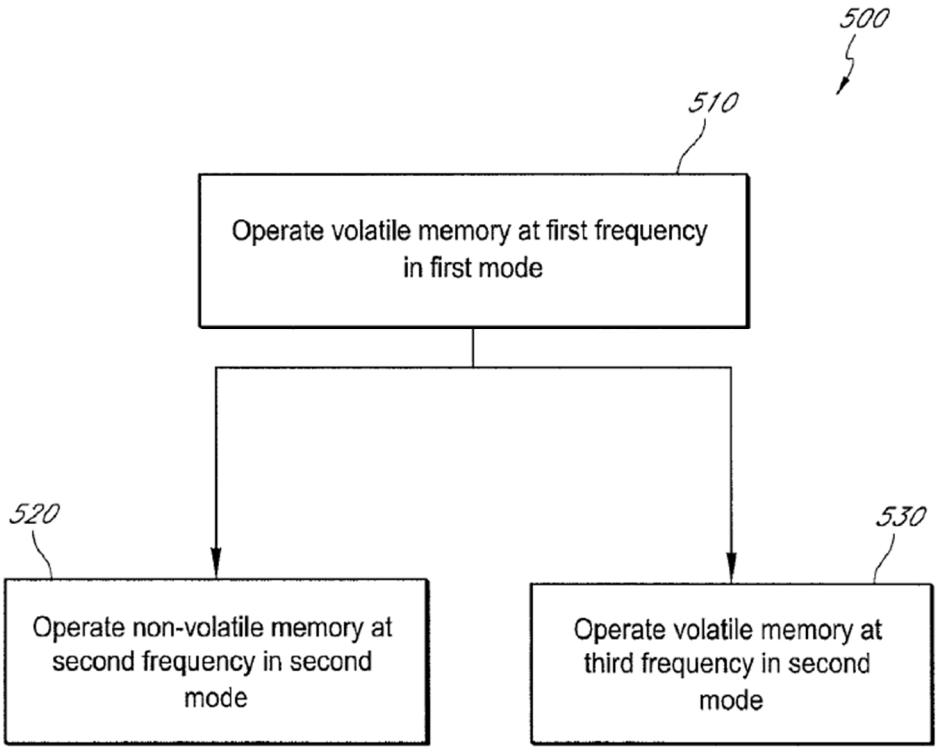


FIG. 9

Id., Fig. 9, 3:45-48; *see id.*, 17:39-18:13; Dec., ¶ 58.

D. Relevant Prosecution History

During prosecution, the claims were initially rejected as obvious in view of the Li and Oshikiri references. Ex. 1002, 166-172. Netlist responded by arguing that the art merely showed "different processing speeds," not "different memory subsystem operation frequenc[ies]." *Id.*, 134-149. The Examiner disagreed, explaining that the claims were "not directed to the operating speed of a memory, but instead … to the operating speed of a memory subsystem." *Id.*, 123. Netlist submitted claim amendments in response, specifying a "first clock frequency," a "second clock frequency," and a "third clock frequency." *Id.*, 107-117.

The claims were again rejected as obvious, over the Li and Cope references. *Id.*, 59-73. The Examiner also rejected what are now claims 2 and 18 as indefinite because they recited "approximately equal" clock frequencies. *Id.* Netlist responded by amending the claims to replace the word "approximately" with "substantially," stating that "in practice there will always be a difference" between clock frequencies. *Id*. Netlistalso argued that Cope "cannot be used to describe two modes of operation, where a DRAM in a first mode operates at a first clock frequency and in a second mode operates at another frequency." *Id.*, 71. The Examiner subsequently withdrew the rejections. *Id.*, 1.

Three previous IPR petitions (by third parties not related to Petitioners) were filed against the '833 Patent. None of these prior petitions involved the Best

(Ex.1006) prior art that Petitioners rely upon as their primary prior art reference herein. In IPR2014-00994, filed by SanDisk Corporation, the Board construed the term "clock frequency" and ultimately denied review of claims 1-30 (Paper 8). In IPR2014-01370, filed by SMART Modular Technologies, the Board denied review of claims 1-30 (Paper 13). In IPR2017-00649, filed by SK hynix, the Board denied review of claims 1-30 (Paper 7).

E. Related Patents

U.S. Patent No. 8,874,831 ("'831 Patent") resulted from Application No. 13/559,476, filed July 26, 2012, a continuation-in-part of the '916 Application (now the '833 Patent). Like the '833 Patent, the '831 Patent alleges a claim of priority to the '586 Application. The '831 Patent's Claim 15, which recites almost verbatim claims 1 and 15 of the '833 Patent, was invalidated in a Final Written Decision by the Board as obvious over Best, Mills, and Bonella. *See SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00692, Paper 25 at 31-40 (PTAB July 5, 2018) ("'692 IPR").[4]

[4] The '692 IPR Final Written Decision also found claim 15 obvious over "Best, Mills, Roy, and Bonella" (Paper 25 at 40), but "Roy" was used to disclose elements not relevant to the present Petition and is not included as a ground herein.

IV. Claim Construction

The Board construes claims under the same standard used in civil actions in federal district court. The district court for the related litigations has not yet construed the claim terms.

The parties' proposed constructions from the related litigations are set forth in Exs. 1012-1013. These construction disputes from the related litigations do not affect the outcome of this Petition with respect to any claim.

The Board has previously construed, under the broadest reasonable interpretation standard, the claim term "*clock frequency*" to require "identification of a clock running at a particular frequency." IPR2014-00994, Paper 8 at 6. This interpretation is consistent with the '833 Patent's specification. *See, e.g.*, Ex. 1001, 17:25-18:13; Dec., ¶ 136. Petitioners have applied this interpretation below and shown how the claims are invalid under any reasonable interpretation of the claim terms.

V. Detailed Discussion of the Grounds for Unpatentability

The Challenged Claims are unpatentable based on two grounds. Ground 1 establishes that claims 1 and 15 are unpatentable under the doctrine of collateral estoppel. Ground 2 establishes that the Challenged Claims are obvious over Best in view of Bonella and Mills.

A. Overview of the Principal Prior Art

1. Best (Ex. 1006)

a. Prior Art Status

Best was filed on October 15, 2009, is related to PCT/US08/60566, filed April 17, 2008, and claims priority to a provisional application (60/912,321) ("'321 Application") (Ex. 1007) filed on April 17, 2007. Best is prior art under 35 U.S.C. § 102(e) (pre-AIA) for two reasons. First, as explained above in §III.A, the earliest effective filing date of the '833 Patent's claims is June 2, 2008. Second, the '321 Application provides written description support for Best's claims, therefore entitling Best to the priority date (April 17, 2007 filing date) of the '321 Application. *See Dynamic Drinkware*, 800 F. 3d at 1381-82. Best is therefore prior art under § 102(e) regardless of whether the '833 Patent is entitled to its alleged June 1, 2007 priority date.

Best and the '321 Application contain essentially identical written descriptions, as can be seen in Appendix A to Mr. Maltiel's report (Ex. 1003). Best's paragraphs correspond to the '321 Application as follows (Dec., ¶ 68):

Best (Ex. 1006)	'321 Application (Ex. 1007)
¶2	¶2
¶¶3-11	¶3
¶¶12-31	¶¶4-23
¶¶32-33	¶24
¶34	¶25

The '321 Application was also filed with the same 40 claims filed in Best, explicitly providing written description support for each claim, and includes the same set of figures. *Compare* Ex. 1006, claims 1-40, Figs. 1-7, *with* Ex. 1007, 27-29 (claims 1-40), 37-38 (Figs. 1-7).

The '321 Application provides written description support for each of Best's claims. Each element of Best's claim 1, for example, has written description support in the '321 Application. For example, the '321 Application discloses:

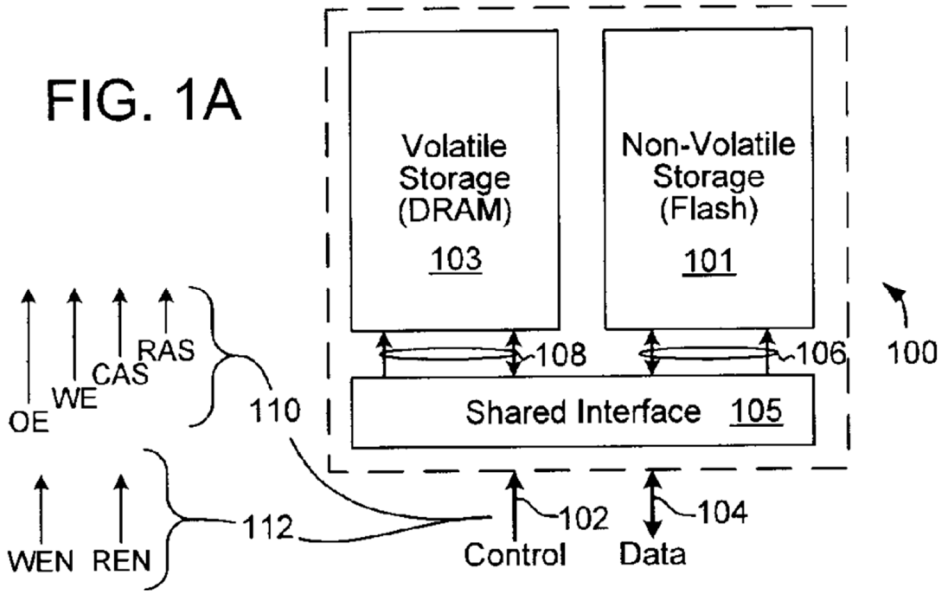
- a "*memory device disposed within an integrated circuit (IC) package*," *see, e.g.*, Ex. 1007, ¶8; Dec., ¶ 71;
- "*a first storage die having an array of volatile storage cells*," *see, e.g.*, Ex. 1007, 37 (Fig. 2); Dec., ¶ 71;
- "*a second storage die having an array of non-volatile storage cells*," *see, e.g.*, Ex. 1007, 37 (Fig. 2); Dec., ¶ 71;
- "*a shared interface circuit to receive information associated with a memory access operation to be performed within the memory device and to select, according to the information, either the first storage die or the second storage die to be accessed in the memory access operation," see, e.g.,* Ex. 1007, ¶¶7, 9; Dec., ¶ 71.

As Dr. Maltiel explains in greater detail in his expert declaration, each of Best's other claims are similarly supported in the '321 Application to the same extent

and same manner as in Best. Dec., ¶¶ 72-111. Best is therefore entitled to the April 17, 2007 filing date of the '321 Application and qualifies as § 102(e) prior art to the '833 Patent.

b. Overview of Best

Best discloses a composite, hybrid memory device including a first volatile storage die and a second non-volatile storage die disposed within an integrated circuit package. Best, Abstract. The device includes a shared interface circuit to receive memory access commands directed to the first storage die and the second storage die and to convey read and write data between an external data path and the first and second storage dice. *Id.* Figure 1A illustrates an embodiment of this hybrid memory device:



Id., Fig. 1A, ¶4; Dec., ¶ 112.

As shown in Figure 1A, the non-volatile storage IC 101 is implemented by a Flash memory die, and the volatile storage IC 103 is implemented by a DRAM die. Best, [0013]. This embodiment is further described by Figures 2 and 3. Dec., ¶¶ 113-114. Best teaches that Figure 3 further describes the embodiment of Figure 2, which itself further describes the embodiment of Figure 1A, such that Figures 1A, 2, and 3 describe a single embodiment. *Id.*, ¶ 114. For example, Figure 1A illustrates "an embodiment of a hybrid, composite memory device 100 having … shared-interface IC 105." Best, [0013]. Figure 1B illustrates an alternative embodiment that puts the location of shared-interface 105 inside the Flash memory, but otherwise the shared interface's functionality is the same. *Id.*, [0016]. Figure 2 "illustrates an embodiment … with *the* shared interface circuitry shown in greater detail," *id.*, [0017] (emphasis added), and thus further describes the shared interface described as part of Figure 1A. Figure 3 "illustrates an embodiment of a data control/steering circuit 150 that may be used to *implement* the data control/steering circuit 131 of FIG. 2." *Id.*, [0021] (emphasis added). Figure 3 (and its associated description) thus further describes the functionality of Figure 2 (and its associated description), which itself further describes the functionality of Figure 1A (and its associated description). Dec., ¶ 114.

Best discloses two alternative ways that memory addresses are mapped to the volatile and non-volatile storage dies. In the Figure 4 hybrid storage embodiment, "non-overlapping address ranges apply to each of the storage dice 101 and 103 to

form" a contiguous address space. Best, [0017]. In the alternative Figure 7 "Shadow Operation" embodiment, "some or all of the volatile memory address range may overlap with the non-volatile memory address range to enable an operation referred to herein as memory shadowing." *Id.*, [0024]. A POSITA would understand that Best's functionality in Figures 1-3 would operate the same in the "Shadow Operation" embodiment except that the address ranges may overlap so as to enable memory shadowing as described. Dec., ¶ 115.

2. Bonella (Ex. 1008)

Bonella, filed on December 8, 2006, claims priority to a provisional application (11/635,926) filed on December 8, 2005. Bonella is thus prior art under 35 U.S.C. § 102(e) (pre-AIA).

Bonella discloses a memory module including a volatile memory, a non-volatile memory, and a controller that provides address, data, and control interfaces to the memories and to a host system, such as, for example, a personal computer. Bonella, [0006]. Bonella teaches that this hybrid memory module fills the performance gap between main memory and a hard disk drive, and "can reduce overall power consumption on laptops." *Id.*, [0065]; Dec., ¶ 118.

Figure 1 is a high-level system block diagram of an illustrative memory module of Bonella:

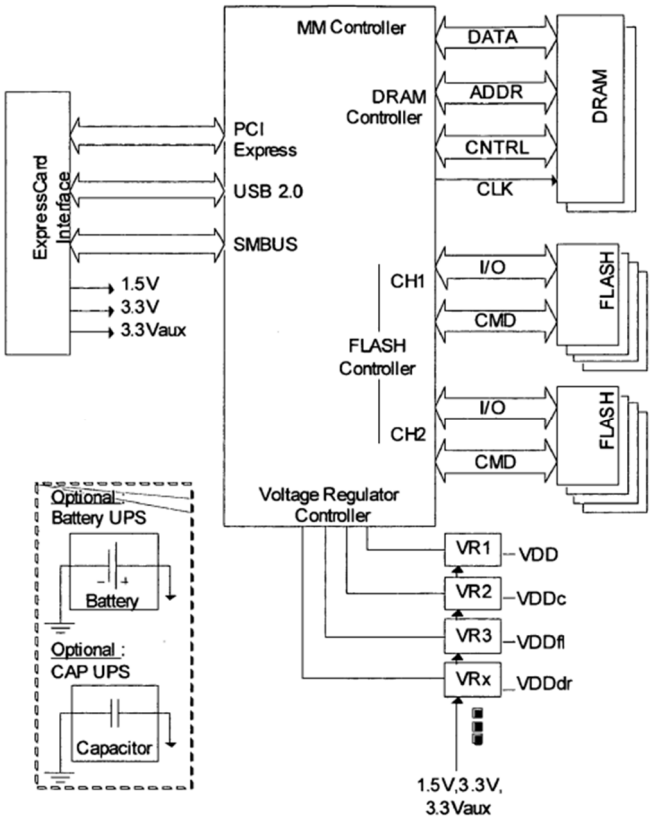


FIG. 1 Memory Module Block Diagram

Figure 1 shows an illustrative memory module with "an Express Card Interface; a memory module controller; a DRAM memory; a FLASH memory; and a voltage regulator (and/or one or more power transistors)," as well as "optional Uninterruptible Power Supply (UPS) capacitors or battery (for emergency shut-down operations); and various other electrical components … used for well-known miscellaneous functions in electronic products such as memory modules." Bonella, [0029]; Dec., ¶¶ 119-120. Bonella discloses that the memory module implements the DDR2 DRAM Specification and the NAND Flash Specification, but can be modified to implement different interfaces and conform with alternative specifications. Bonella, [0036]-[0037]; Dec., ¶ 121.

Bonella teaches that using a combination of storage types can "gain dramatic improvements in operational performance and storage capacity," but that doing so requires "special embedded operational functions" in order to allow the memory module to operate independently so as to limit interference with normal system operation. Bonella, [0025]. These functions include Flash write leveling, DRAM write buffer flushing to Flash, Flash flushing to HDD, device failure management, a power loss algorithm, security management, etc. *Id.*, [0092]-[0108]; Dec., ¶ 122.

Bonella teaches that its hybrid memory includes a DRAM write buffer that is occasionally backed up to the internal Flash memory to ensure data integrity in case of a power loss. *Id.*, [0096]. This write buffer flushing can be triggered by a power loss event, which then causes Bonella's "Power loss algorithm" to be executed. *Id.*, [0101]. During the execution of the power loss algorithm, Bonella's memory relies on backup power such as, for example, power supply capacitors. *Id.*, [0029]. The memory maintains a sufficiently large power reserve to write the data to Flash memory. *Id.*, [0033]; Dec., ¶¶ 123-126.

Bonella also teaches that the hybrid memory module includes "Power State Aware" functionality that allows the module to significantly reduce power consumption when required. Bonella, [0045]. For example, Bonella teaches a "Power Level 5" state that allows for full function, full performance operation. *Id.*, [0047]. Bonella also teaches a "Power Level 4" state that reduces the power

consumption of the memory module by limiting the DRAM performance. *Id.*, [0048]. Bonella explains that one way to reduce the power consumption of the memory module is to slow or reduce the operating frequency of the DRAM. *Id.*, [0049]-[0050]; Dec., ¶¶ 127-130. Bonella teaches that reducing the DRAM frequency in this way can result in "major power savings." Bonella, [0050].

3. Mills (Ex. 1009)

Mills was issued on February 15, 2000, and is therefore prior art under 35 U.S.C. § 102(b) (pre-AIA). Mills describes several interfaces for a Flash memory device, one of which is a synchronous flash interface: "FIG. 6 illustrates a block diagram of a synchronous flash interface (SFI) flash memory integrated circuit 600 that incorporates a complete synchronous flash interface in a single flash memory chip." Mills, 16:60-63. The synchronous flash interface includes a clock input such that all the external operations of the device are synchronized to the rising edge of the clock. *Id.*, 17:10-25.

Mills teaches that this synchronous operation is used for both read operations and write operations: "When SFI is enabled, interlace control 670 and [bank] select logic 674 operate to interlace read (and write) operations between flash bank A 610 and a flash bank B 620 …." *Id.*, 17:33-39. Because "the device is interleaved internally," it "creates an average access time for sequential read accesses that is

significantly less than the access time of an asynchronous flash device." *Id.*, 17:1-9; Dec., ¶¶ 132-133.

B. Ground 1: Under the Doctrine of Collateral Estoppel, Claims 1 and 15 are Unpatentable and Netlistis Estopped From Relitigating those Adjudicated Issues

Whether or not claims 1 and 15 are unpatentable is not open for discussion. The PTAB previously invalidated claim 15 of the '831 Patent—a claim that is substantively identical, in relevant part, to claims 1 and 15 of the '833 Patent. *See* '692 IPR at 40 ("[W]e are persuaded … that claim 15 of the '831 patent [is] unpatentable under 35 U.S.C. § 103(a) as obvious over Best, Mills, and Bonella."). As a result, as detailed below, claims 1 and 15 are unpatentable under the doctrine of collateral estoppel based on that final adjudicative decision in the '692 IPR that claim 15 of the '831 Patent is unpatentable. "[T]he collateral-estoppel effect of an administrative decision of unpatentability generally requires the invalidation of related claims that present identical issues of patentability." *MaxLinear, Inc. v. CF CRESPE LLC*, 880 F.3d 1373, 1377 (Fed. Cir. 2018). Additionally, Netlistis estopped from relitigating the issue of validity of claims 1 and 15. "Collateral estoppel protects a party from having to litigate issues that have been fully and fairly tried in a previous action and adversely resolved against a party-opponent." *Ohio Willow Wood Co. v. Alps South, LLC*, 735 F.3d 1333, 1342 (Fed. Cir. 2013).

The Federal Circuit has established that: "[a] party is collaterally estopped from relitigating an issue if:

(1) a prior action presents an identical issue;

(2) the prior action actually litigated and adjudged that issue;

(3) the judgment in that prior action necessarily required determination of the identical issue; and

(4) the prior action featured full representation of the estopped party."

VirnetX Inc. v. Apple, Inc., 909 F.3d 1375, 1377 (Fed. Cir. 2018). The Federal Circuit has made clear that collateral estoppel applies in the context of *inter partes* reviews. *MaxLinear*, 880 F.3d at 1376. And the PTAB has applied collateral estoppel to estop re-litigation of previously-adjudged issues. *See, e.g.*, *Thorne Research, Inc. v. Trustees of Dartmouth College*, IPR2021-00268, Paper 21 at 11-13 (PTAB June 10, 2021) (applying collateral estoppel to stop relitigating validity of previously-invalidated claim); *Nevro Corp. v. Boston Scientific Neuromodulation Corp.*, IPR2019-01313, Paper 74 at 56-58 (PTAB January 19, 2021) (applying collateral estoppel to stop re-argument of issue rejected in a previous IPR); *Rimfrost AS v. Aker Biomarine Antarctic AS*, IPR2018-01730, Paper 35 at 21-24 (PTAB March 6, 2020) (applying collateral estoppel even though the previous "decisions addressed different patents and claims"); *RimFrost AS v. Aker Biomarine Antarctic AS*,

IPR2018-01178, Paper 34 at 32 (PTAB Jan. 13, 2020) (applying estoppel to issues adjudged in prior IPRs involving related patent).

Here, all factors of the collateral estoppel test are met and support a finding that challenged claims 1 and 15 of the '833 Patent are unpatentable. The relevant prior action is the '692 IPR. As to factor (1), the issue of whether claims 1 and 15 of the '833 Patent are unpatentable is identical to the issue of whether claim 15 of the '831 Patent is unpatentable, the latter being an issue already adjudicated in the '692 IPR. In particular, the substantive features of challenged claims 1 and 15 of the '833 Patent are materially identical to the substantive features of unpatentable claim 15 of the '831 Patent. To illustrate, the below claim comparison chart shows that claim 1 of the '833 Patent and claim 15 of the '831 Patent are materially indistinguishable.[5]

Claim 1 of '833 Patent (Challenged Claim)	**Claim 15 of '831 Patent (Adjudged Unpatentable)**
1. A method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:	7. A method for managing a memory module by a memory controller, the memory module including volatile and non-volatile memory subsystems, the method comprising: …

[5] A chart is not provided comparing the '833 Patent's claim 15 to the '831 Patent's claim 15 because such a chart is redundant of the provided chart, i.e., there is no material difference between claim 1 of the '833 Patent (a "method" claim), claim 15 of the '833 Patent (a "memory system" claim), and claim 15 of the '831 Patent.

	15. The method of claim 7, further comprising:
operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;	operating the volatile memory subsystem at a first clock frequency when the memory module is in a first mode of operation in which data is communicated between the volatile memory subsystem and the memory controller;
operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and	operating the non-volatile memory subsystem at a second clock frequency when the memory module is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and
operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.	operating the volatile memory subsystem at a third clock frequency when the memory module is in the second mode of operation, the third clock frequency being less than the first clock frequency.

That claim 1 (or claim 15) of the ’833 Patent and unpatentable claim 15 of the ’831 Patent are not verbatim identical does not preclude application of collateral estoppel. Specifically, it is well settled that a ruling on an issue, e.g., patent claim validity, in a prior judgment can have preclusive effect even if the issue is raised in a later case involving different patents and different claims. *See Ohio Willow*, 735 F.3d at 1342. The patent claims need not be verbatim identical, but “substantially similar” so that the issues of validity are materially the same. *Id*. Indeed, “it is the identity of the issues that were litigated that determines whether collateral estoppel

should apply." *Id*. "If the differences between the unadjudicated patent claims and adjudicated patent claims do not materially alter the question of invalidity, collateral estoppel applies." *Id*. Here, the only difference between claim 1 (or claim 15) of the '833 Patent and unpatentable claim 15 of the '831 Patent is the very slight difference in a few words used to describe the same invention. But "the mere use of different words in these portions of the claims does not create a new issue of invalidity." *Id*. at 1343. Indeed, "'merely because the invention … is presented in varying language or varying combinations of elements does not necessarily mean that the issues bearing on nonobviousness of that concept or contribution vary from one claim to the next.'" *Mobile Tech, Inc. v. InVue Security Products Inc.*, IPR2018-01138, Paper 28 at 29 (PTAB Dec. 5, 2019).

Not only is the claim language materially identical, but the prior art references, and supporting arguments, asserted here against claims 1 and 15 of the '833 Patent are also identical to the prior art references, and supporting arguments, evaluated by the PTAB in the '692 IPR to render claim 15 of the '831 Patent unpatentable. *Compare* §V.C.1, below, *with* the '692 IPR at 31-40 (§II.H). And the PTAB has applied collateral estoppel where, as is the case here, a later IPR and a prior action involve "materially similar issues, including the same prior art, materially similar claims, and materially similar arguments," albeit in different patents. *Amazon.com, Inc. v. M2M Solutions LLC*, IPR2019-01204, Paper 43 at 11 (PTAB January 20,

2021); *see also Thorne Research*, IPR2021-00268, Paper 21 at 12. Indeed, "[i]t has long been understood that a party may be bound not simply by the ultimate conclusion (e.g., unpatentability of a claim), but by any subsidiary factual determinations that were actually litigated and essential to the judgment." *Mobile Tech*, IPR2018-01138, Paper 28 at 20-21.

In view of the foregoing, the first collateral estoppel factor—"(1) a prior action presents an identical issue"—is met.

It is equally undisputable that the remaining collateral estoppel factors are met. First, as to factors (2) and (3), the parties in the '692 IPR, including Netlist, fully briefed the raised validity issue of claim 15 of the '831 Patent, as well as the necessary sub-issues. Based on that briefing and oral arguments by the parties, the PTAB issued a final written decision holding claim 15 of the '831 Patent to be unpatentable. Thus, there can be no dispute that the ultimate issue of validity of claim 15 of the '831 Patent was actually litigated and adjudged in the '692 IPR, as well as the sub-issues pertaining to the same prior art, materially similar specific claim features, and materially similar arguments. Also, the invalidity holding of claim 15 of the '831 Patent undoubtedly "necessarily required determination of the identical issue" of the validity of claim 15 of the '831 Patent because the validity of claim 15 of the '831 Patent was the only issue litigated in the '692 IPR with respect to that claim. And the finality of the holding in the '692 IPR final written decision for

collateral estoppel purposes is also undisputable as Netlist did not appeal that decision and the time for appeal has expired.

Finally, as to factor (4), Netlist was fully represented by counsel in the '692 IPR and "has not argued or suggested that it was not adequately represented." *Thorne Research*, IPR2021-00268, Paper 21 at 12.

As shown, all factors of the collateral estoppel test are met. Accordingly, challenged claims 1 and 15 are unpatentable under the doctrine of collateral estoppel, and Netlist is estopped from re-litigating the issue of validity of claims 1 and 15 of the '833 Patent.

C. Ground 2: Claims 1, 3-17, and 19-30 Are Obvious Over Best in View of Bonella and Mills

1. Claims 1 and 15

Even if the Board does not apply collateral estoppel to find claims 1 and 15 unpatentable based on the holding in the '692 IPR that claim 15 of the '831 Patent is unpatentable, the Board should still be guided by the underlying rationale for that holding. That is, the '692 IPR provides informative guidance for the Board's analysis of challenged claims 1 and 15 in this case, and the Board should not depart from its prior holding that claim 15 of the '831 Patent is unpatentable, nor from the underlying rationale for that holding.

Thus, as shown below, for the same reasons that the PTAB found claim 15 of the '831 Patent unpatentable in the '692 IPR, claims 1 and 15 of the '833 Patent are unpatentable as obvious over Best, Bonella, and Mills.

a. Preambles

The preamble of claim 1 recites *"[a] method for controlling a memory system operatively coupled to a host system*." The preamble of claim 15 recites "*[a] memory system operatively coupled to a host system*."

Best discloses a "hybrid, composite memory device having non-volatile and volatile memories implemented in distinct integrated circuit (IC) dice that are packaged together and accessed through a shared interface." Best, [0012]-[0017], Fig. 2; Dec., ¶¶ 140-142. The memory device includes DRAM die 103, Flash memory die 101, and shared interface circuitry including, e.g., "an external request interface 125, external data interface 133, command decoder 122, address queue 135, DRAM control circuit 129, Flash control circuit 137, and data control/steering circuit 131." Best, [0017]. "[I]ncoming control signals and addresses … are received in the external request interface 125 via control/address (CA) path 126 and then forwarded to the command decoder 122." *Id.* This memory device ("*memory system*") includes an interface that "receive[s] commands from a controller device (not shown in FIG. 1A)," ("*operatively coupled to a host system*"). *Id.*, [0014]; Dec., ¶ 142. Best discloses techniques for using the shared interface to control access by

the controller device to the non-volatile and/or volatile memories ("*[a] method for controlling a memory system operatively coupled to a host system*"). Best, [0012]-[0017], Fig. 2; Dec., ¶¶ 140-142.

Therefore, these claim elements are obvious.

b. Operating a "Volatile Memory Subsystem" at a "First Clock Frequency"

Claim 15 recites that the memory system comprises "*a volatile memory subsystem operable at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system*." The preamble of claim 1 recites that the memory system includes "*a volatile memory subsystem*," and claim 1 further recites that the method comprises "*operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system*."

Best discloses a "*volatile memory subsystem*" in the form of a DRAM. Best, [0017], [0021]. This is so under any reasonable interpretation of the claim term "*volatile memory subsystem*," including under an ordinary and customary meaning of the term and under both Petitioners' and Netlist's proposed constructions for the term. Dec., ¶ 145.

Best further discloses "*a volatile memory subsystem operable at a first clock frequency*." Best explains that the volatile memory die ("*volatile memory*

subsystem") can be synchronous or asynchronous, and explains that a conventional synchronous DRAM interface relies on "clock and clock-enable signals." Best, [0014]. A POSITA would have understood this disclosure to mean that a synchronous DRAM is "*operable at a first clock frequency*" because it is operated synchronously by a clock signal. Dec., ¶¶ 146-147. This corresponds to the usual operation of DRAM memory, as would have been well-known by a POSITA. *Id.* For example, according to the DDR2 specification at the time of Best's priority date, a conforming DDR2 DRAM device receives two input clock signals. DDR2 SDRAM Specification, JESD79-2B (Jan. 2005) (Ex. 1017), 6, 29. A POSITA would thus understand Best's DRAM to be operated by a clock signal at a particular frequency. Dec., ¶¶ 146-147.

Best also discloses "*a first mode of operation in which data is communicated between the volatile memory subsystem and the host system*." Best discloses a "Shadow Operation" embodiment where a portion of the DRAM is used as a write buffer for the non-volatile memory. Best, [0024]; Dec., ¶ 148. "[D]ata is stored in a fast-access volatile storage die," and later "a write-back trigger is detected within the shared interface circuitry," such as a "power-loss" event. Best, [0025]-[0026]. Once the power-loss event is detected, "internal data transfer operations are performed to transfer data … from the DRAM to … the NV memory." *Id.*; Dec., ¶ 148.

Best therefore describes at least two modes of operation: (1) the operation of the system when no write-back trigger is detected ("*a first mode of operation*"), and (2) the operation of the system when a power-loss event write-back trigger is detected ("*a second mode of operation*"). Best, [0025]-[0026]; Dec., ¶¶ 148-150. As noted above, the DRAM ("*volatile memory subsystem*") would normally be operated at a particular clock frequency of operation in accordance with "clock and clock-enable signals." Best, [0014]; Dec., ¶¶ 146-147, 151-152. Therefore, Best discloses that the "*volatile memory subsystem [is] operable at a first clock frequency when the memory system is in a first mode of operation*." Dec., ¶ 149.

Best's "*first mode of operation*" (i.e., the operation of the system when no write-back trigger is detected) is one in which "*data is communicated between the volatile memory subsystem and the host system*" because initially "data is stored in a fast-access volatile storage die" and only later after a write-back trigger is written to non-volatile memory. Best, [0025]; Dec., ¶¶ 148-150.

To the extent one might argue that the Board's interpretation of "*clock frequency*" requires a particular numeric value (i.e., as in number of cycles per second), it would have been obvious to operate Best's DRAM at any of the frequencies described by the DDR DRAM and DDR2 DRAM standards, e.g., 67-400MHz. Dec., ¶ 151 (discussing Ex. 1018, 62; Ex. 1017, 77). Best teaches that "any [] type of volatile storage technology may be used …." Best, [0013]-[0014]. It would

have been obvious to use one of the known DDR or DDR2 DRAM modules in Best's system, and to subsequently clock the module at its standards-specified rate. Dec., ¶ 152. To do so would have been merely the use of a known structure (a standard DRAM module and clock frequency) for its known use (operation as a DRAM module) to achieve a predictable result (operating a DRAM module at a standard clock frequency in Best's system). *Id.* A POSITA would have been motivated to operate DDR2 DRAM at those frequencies in order to ensure proper operations of the memory. *Id.* Therefore, operating Best's volatile memory "*at a first clock frequency*" would have been obvious.

Therefore, these claim elements are obvious.

c. Operating a "Non-Volatile Memory Subsystem" at a "Second Clock Frequency"

Claim 15 recites that the memory system comprises "*a non-volatile memory subsystem operable at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem*." The preamble of claim 1 recites that the memory system includes "*a non-volatile memory subsystem*," and claim 1 further recites that the method comprises "*operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem*."

Best discloses a "*non-volatile memory subsystem*" in the form of a Flash memory. Best, [0017]. The Flash memory can be "NAND-Flash or NOR-Flash" or "any other electrically-erasable or electrically-alterable storage technology." *Id.*, [0013]; Dec., ¶ 155. Best discloses the "*non-volatile memory subsystem*" under any reasonable interpretation of the claim term "*non-volatile memory subsystem*," including under an ordinary and customary meaning of the term and under both Petitioners' and Netlist's proposed constructions for the term. Dec., ¶ 155.

Best also discloses "*a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem*." Best discloses a "Shadow Operation" embodiment where a portion of the DRAM is used as a write buffer for the non-volatile memory. Best, [0024]; Dec., ¶ 156. "[D]ata is stored in a fast-access volatile storage die," and later "a write-back trigger is detected within the shared interface circuitry," such as a "power-loss" event. Best, [0025]-[0026]. Once the power-loss event is detected, "internal data transfer operations are performed to transfer data … from the DRAM to … the NV memory." *Id.*; Dec., ¶ 156.

Best therefore describes at least two modes of operation: (1) the operation of the system when no write-back trigger is detected ("*a first mode of operation*"), and (2) the operation of the system when a power-loss event write-back trigger is detected such as a power-loss ("*a second mode of operation*"). Best, [0025]-[0026];

Dec., ¶¶ 156-158. Best's "*second mode of operation*" (i.e., the operation of the system when a power-loss write-back trigger is detected) involves "*a non-volatile memory subsystem operable*" (Best's "NV" memory) such that "*data is communicated between the volatile memory subsystem and the non-volatile memory subsystem*," e.g., when "internal data transfer operations are performed to transfer data … from the DRAM to … the NV memory." Best, [0025]-[0026]; Dec., ¶¶ 156-158.

Best does not explicitly disclose "*operating the non-volatile memory subsystem*" (the Flash memory) "*at a second clock frequency*" during this second mode, but it would have been obvious to include that functionality in the system of Best. Dec., ¶ 159.

Synchronous Flash memory interfaces that were operated by clock signals were well-known in the art by the '833 Patent's priority date. Dec., ¶ 160. One prior art Flash implementation is described by Mills (Ex. 1009), which describes a synchronous flash interface: "FIG. 6 illustrates a block diagram of a synchronous flash interface (SFI) flash memory integrated circuit 600 that incorporates a complete synchronous flash interface in a single flash memory chip." Mills, 16:60-63. The synchronous flash interface causes the Flash memory system to "*opera[te] at a second clock frequency*": "A clock input is a part of the interface. … All the external operations of the device are synchronized to the rising edge of the clock. …

The user can cycle the device at frequencies as high as 33 MHz." *Id.*, 17:10-25; Dec., ¶ 160.

Mills teaches that this synchronous operation is used for both read operations and write operations: "When SFI is enabled, interlace control 670 and [bank] select logic 674 operate to interlace read (*and write*) operations between flash bank A 610 and a flash bank B 620." Mills, 17:28-39 (emphasis added). Because "the device is interleaved internally," "this interface creates an average access time for sequential read accesses that is significantly less than the access time of an asynchronous flash device." *Id.*, 17:1-9. Mills therefore teaches a POSITA a synchronous Flash interface where read and write operations are synchronized to the rising edge of a clock signal provided to the device and operating at a particular frequency (i.e., "*a non-volatile memory subsystem operable at a second clock frequency*"). Dec., ¶ 161. To the extent one might argue that the Board's interpretation of "*clock frequency*" requires a particular numeric value (i.e., as in number of cycles per second), Mills discloses the use of his Flash memory at, for example, a frequency "as high as 33 MHz." Mills, 17:10-25; Dec., ¶ 167.

Best and Mills are both analogous art to the '833 Patent because each is from the field of memory systems. Ex. 1001, 3:60-63; Best, [0001]; Mills, 6:57-59; Dec., ¶ 162. As of the priority date of the '833 Patent, it would have been obvious to a POSITA to employ a synchronous flash memory, such as disclosed in Mills, in the

system of Best because to do so would have been merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement, i.e., the non-volatile storage of data. Dec., ¶ 163.

As combined, Best's Flash interface would conform to Mills' synchronous Flash protocol and include a separate clock signal that controls read and write operations. Mills, 17:10-25, 17:28-39. This means that Best's Flash memory ("*non-volatile memory subsystem*") would operate at "*a second clock frequency*," i.e., the frequency of the synchronous Flash interface clock up to 33 MHz (Mills, 17:10-25), during its operation, including when a write-back trigger is detected and data is written from DRAM to Flash ("*when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem*"). Dec., ¶ 164.

A POSITA would have been motivated to make such a combination because, as Mills explains, a synchronous flash interface "creates an average access time for sequential read accesses that is significantly less than the access time of an asynchronous flash device." Mills, 17:6-9. In the context of Best, restoring data from the non-volatile flash memory would therefore have been faster by use of a synchronous flash memory, and reduced sequential read access times during other

operations or uses of Best's Flash memory, motivating a POSITA to use a synchronous interface generally. Dec., ¶ 165.

Moreover, Best discloses that his "non-volatile storage IC 101 … is implemented by a Flash memory die … of either the NAND-Flash or NOR-Flash varieties, though any other electrically-erasable or electrically-alterable storage technology may alternatively be used." Best, [0013]. A POSITA would have therefore understood Best to suggest modification to work with any known Flash interface, including Mills' synchronous Flash interface. Dec., ¶ 166.

Therefore, these claim elements are obvious.

d. Operating the "Volatile Memory Subsystem" at a "Third Clock Frequency"

Claim 1 recites that the method further comprises "*operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency*." Claim 15 recites "*the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency*."[6]

[6] The phrase "*clock first frequency*" appears to be a typographical error that should read "*first clock frequency*." Dec., ¶ 169 n.6. For the purposes of this Petition only, Petitioner asserts that "*clock first frequency*" means "*first clock frequency*."

As explained above, Best discloses or renders obvious "*a volatile memory subsystem operable at a first clock frequency*," but does not explicitly disclose the "*volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the [first clock] frequency*." Dec., ¶¶ 146-152. Doing so, however, would have been obvious at the time of the '833 Patent's priority date for two reasons: (1) reducing power during volatile to non-volatile flush operations prompted by a power loss was a well-known technique, and (2) one known way to reduce the power consumption of DRAM devices was to reduce their frequency of operation. *Id.*, ¶ 170. It would have therefore been obvious to operate Best's DRAM "*at a third clock frequency*" that is "*less than the [first clock] frequency*" when performing Best's flush operation (i.e., "*when the memory system is in the second mode of operation*"). *Id.*

First, reducing power consumption during memory backup operations initiated in response to an interrupted power supply was known by the priority date of the '833 Patent, as were its advantages. For example, Ashmore (Ex. 1010) "reduc[es] battery power consumption during a main power loss to reduce the likelihood of loss of user write-cached data in a write-caching mass storage controller." Ex. 1010, ¶9; Dec., ¶ 171. As another example, Long (Ex. 1011), discloses that "if there is a loss of primary power 34, … a significantly slower clock

signal [is provided] to … the controller 40 while the controller 40 moves data from the volatile-memory storage cache 42 to the flash-based memory vault 44." Ex. 1011, 4:54-64. "As a result, less power is consumed thus enabling the use of a smaller-sized backup power source 28 (e.g., a relatively small battery)." *Id.* Reducing power consumption during memory backup operations initiated in response to an interrupted power supply was therefore well-known and would reduce the likelihood of data loss or reduce the necessary size for the backup power source. Dec., ¶ 172.

A POSITA would have been motivated to reduce the power consumption during Best's write flushing in response to a power loss. A POSITA would have been motivated to perform this power reduction technique for all the reasons that were known in the art: e.g., decreasing the risk of data loss due to insufficient backup power (Ex. 1010, ¶7) and enabling the use of a smaller-sized backup power source (Ex. 1011, 4:54-64). Reducing power consumption during write flushing in response to a power loss would also have been the arrangement of old elements, each performing the same function it had been known to perform, in a way that yields no more than a POSITA would expect from such an arrangement (reducing power consumption during a power loss event, as suggested by Long and Ashmore). Dec., ¶ 173.

Second, it was known that one way to reduce the power consumption of a DRAM was to reduce the operating frequency of the DRAM, i.e., by lowering its clock frequency. For example, Bonella (Ex. 1008) explains that one way to reduce the power consumption of the memory module is to slow or reduce the operating frequency of the DRAM. Bonella, [0049]-[0050]; Dec., ¶ 174. Best and Bonella are both analogous art to the '833 Patent because each is from the field of memory systems. Ex. 1001, 3:60-63; Best, [0001]; Bonella, [0002]; Dec., ¶ 175.

A POSITA would also have found it obvious to reduce power consumption during Best's write flushing in response to a power loss using any known or conventional means, and would have also considered power consumption reduction techniques other than those of Ashmore and Long to obtain the same benefits, including those described in Bonella. Bonella describes reducing the operational frequency of the DRAM in order to reduce the power consumption generally. Bonella, [0050]. An ordinary artisan would have found it obvious to perform Bonella's power reduction technique (DRAM operational frequency reduction) during the performance of Best's write flushing in response to a power loss, in view of the specific motivations evidenced by Ashmore and Long. Dec., ¶ 176.

Bonella also motivates the use of his technique because it results in "major power savings." Bonella, [0050]. Using Bonella's power reduction technique during Best's write flushing would also have been the arrangement of old elements, each

performing the same function it had been known to perform, in a way that yields no more than a POSITA would expect from such an arrangement (reducing power consumption during a power loss event, as suggested by Long and Ashmore). Dec., ¶ 177.

Reducing the DRAM's operational frequency in such a situation would not have caused any performance issues because the transfer of data between DRAM and FLASH could not occur faster than the speed of the FLASH, which in the case of Best would be substantially slower than the DRAM. Best, [0002], [0012], [0018]; Dec., ¶ 178. Bonella teaches that various levels of a computer's memory hierarchy have different performance levels, and lists DRAM as higher performance than Flash memory. Bonella, [0065], Fig. 3; Dec., ¶ 178. A POSITA would have understood that reducing the DRAM operating frequency in this way would not cause performance issues. Dec., ¶ 178. Such a modification would have therefore been obvious.

In light of the foregoing, claims 1 and 15 are unpatentable as obvious over Best, Bonella, and Mills.

2. Claim 16

Claim 16 depends on claim 15 and recites that the memory system further comprises "*a controller configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation and to couple the*

non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation."

Best discloses "*a controller*" in the form of a shared interface circuit. Best, [0012]; Dec., ¶ 181. Specifically, Best discloses that the "memory device ha[s] nonvolatile and volatile memories implemented in distinct integrated circuit (IC) dice that are packaged together and accessed through a shared interface." Best, [0012], [0017], Figs. 2-3. The shared interface circuitry includes, e.g., "an external request interface 125, external data interface 133, command decoder 122, address queue 135, DRAM control circuit 129, Flash control circuit 137, and data control/steering circuit 131." *Id.*, [0017]. The shared interface circuitry also includes, as part of the data control/steering circuit 131/150, "data control circuit 151, multiplexer 153, secondary volatile and non-volatile data paths 155 and 157 (secondary as opposed to primary volatile and non-volatile data paths 142 and 144), volatile-storage-die interface buffer 159, non-volatile-storage-die interface buffer 161, and inter-die data path 171." *Id.*, [0021].

Best also discloses that the shared interface circuitry ("*controller*") is "*configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation*." Dec., ¶ 182. As described with respect to claim 15, "*the first mode of operation*" may correspond to the operation of Best's system when no write-back trigger is detected, such as when "data [is

initially] stored in a fast-access volatile storage die." Best, [0025]-[0026]; Dec., ¶ 182. Best discloses or renders obvious that during this first mode of operation, the Flash memory is decoupled from the DRAM because during "a memory write operation" when no write-back trigger has yet been detected, "data received via shared internal data path 140 is passed, via multiplexer 153, to **one** of the secondary data paths 155, 157 according to the memory access target (e.g., indicated by memory-select signal MSel as described in reference to FIG. 4)." Best, [0021], [0025], [0017]; Dec., ¶ 183. In other words, during this first mode of operation, access to only one of the DRAM or the Flash memory is enabled, and when access to one is enabled access to the other is not enabled. Best, [0017], [0021]-[0022], [0025]; Dec., ¶ 183. For example, Best discloses that during the first mode of operation, i.e., no write-back trigger yet detected, "[i]f the volatile storage die 103 is the target of the memory write, the data control circuit 151 switches the multiplexer 153 to convey data from the shared internal path 140 to secondary data path 155, and signals the DRAM interface buffer 159 to enable the data to be buffered (or queued) therein for eventual transfer to the DRAM die via data path 142." Best, [0021]; Dec., ¶ 183. By contrast, "in a memory write operation directed to the non-volatile storage die 101, the data control circuit 151 switches the multiplexer 153 to convey data from the shared internal path 140 to secondary data path 157 and signals the non-volatile-die interface buffer 161 to enable the data to be buffered (or queued)

therein for eventual transfer to the non-volatile storage die via data path 144." Best, [0022]. Best further discloses that a comparator may be used to provide the signals that enable the different data paths, and that "the most significant bit of the incoming address (e.g., 0=DRAM, 1=Flash) … may be used [by the comparator] to enable access to either the volatile storage die or non-volatile storage die." *Id.*, [0017]; Dec., ¶ 184. That is, the DRAM data path and the Flash data path are not enabled at the same time. Dec., ¶ 184.

Best further discloses that the shared interface circuitry ("*controller*") is "*configured … to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation*." *Id.*, ¶ 186. As described with respect to claim 15, "*the second mode of operation*" may correspond to the operation of Best's system when a power-loss event write-back trigger is detected, e.g., a memory shadow operation in which "internal data transfer operations are performed to transfer data … from the DRAM to … the NV memory." Best, [0025]-[0026]; Dec., ¶ 186. Best discloses or renders obvious that during this second mode of operation, the Flash memory is coupled to the DRAM so that "the data read out of the volatile storage die may be transferred from the volatile-die interface buffer 159 to the non-volatile-die interface buffer 161 via the inter-die data path 171. The transferred data may then be stored in the non-volatile storage die to implement a memory shadowing function." Best, [0021]; Dec., ¶ 187. Best therefore discloses that at least the

following elements of the shared interface circuitry couple the Flash memory to the DRAM: volatile-die interface buffer 159, non-volatile-die interface buffer 161, and inter-die data path 171. Best, [0021]; Dec., ¶ 187.

A POSITA would have understood the foregoing disclosure from Best to disclose or render obvious claim 16. Dec., ¶¶ 185, 188. Therefore, Best discloses or renders obvious claim 16 under any reasonable interpretation of claim 16, including under an ordinary and customary meaning of claim 16 and under both Micron's and Netlist's proposed constructions for claim 16. Dec., ¶ 189. Accordingly, claim 16 is unpatentable as obvious over Best, Bonella, and Mills.

3. Claim 17

Claim 17 depends on claim 15 and further recites "*a plurality of power supplies and a switch configured to selectively deliver power from the plurality of power supplies to the volatile memory subsystem and the non-volatile memory subsystem as a function of the mode of operation.*"

Best does not explicitly disclose the foregoing features of claim 17, but it would have been obvious, in light of Bonella, to include those features in the system of Best. Dec., ¶ 191.

In particular, the features of claim 17 were well-known in the art by the '833 Patent's priority date. *Id.*, ¶ 192. For example, Bonella discloses that the memory module is provided a standard power source and also a backup power source ("*a*

plurality of power supplies"). Bonella, [0033]; Dec., ¶ 192. Bonella's system selectively delivers power from one of these power sources depending on whether it is operating conventionally ("*first mode*") or is responding to a power loss event ("*second mode*"). Bonella, [0101], [0033]; Dec., ¶ 192. Bonella's power functionality as a whole operates to fulfill the claimed "*switch*" because it switches between the standard power source to the backup power source when necessary. Dec., ¶ 192; *see, e.g.*, Bonella, [0029]-[0031], 101. Indeed, Bonella discloses that its power functionality includes "one or more power transistors," which a POSITA would have understood to refer to "*switch[es]*" that are coupled to the available power sources and that are each configured to, when enabled, allow their associated power source to deliver power to the components of the memory module. Bonella, [0029]; Dec., ¶ 192.

Best and Bonella are both analogous art to the '833 Patent because each is from the field of memory systems. Ex. 1001, 3:60-63; Best, [0001]; Bonella, [0002]; Dec., ¶ 193.

As of the priority date of the '833 Patent, it would have been obvious to a POSITA to include Bonella's power supplies and associated selective power switching functionality/circuitry, including the power transistors, in Best's hybrid memory devices because to do so would have been merely an arrangement of old elements (Best's hybrid memory device system and Bonella's power supplies and

associated selective power switching functionality/circuitry), each performing the same function it had been known to perform (Bonella's power supplies and associated power switching functionality/circuitry being used to switch power in Best's system), in a way that yields no more than a POSITA would expect from such an arrangement (Bonella's power switching used in Best's hybrid memory device system to selectively deliver power to the components in Best's system). Best, [0025]-[0026]; Bonella, [0029]-[0031], [0033], [0101]; Dec., ¶ 194. As shown here, such a combination would have been obvious.

Therefore, Bonella discloses or renders obvious claim 17, and claim 17 is unpatentable as obvious over Best, Bonella, and Mills.

4. Claims 3 and 19

Claims 3 and 19 depend on claims 1 and 15, respectively, and further recite "*wherein the memory system is not powered by a battery when it is in the second mode of operation*." The '833 Patent provides "a capacitor" as an example of a non-battery power source. Ex. 1001, 4:2-4.

Best does not explicitly disclose the foregoing features of claims 3 and 19, but it would have been obvious, in light of Bonella, to include those features in the system of Best. Dec., ¶ 197.

In particular, the features of claims 3 and 19 were well-known in the art by the '833 Patent's priority date. *Id.*, ¶ 198. For example, Bonella explains that the

power loss event is powered by either a battery or capacitors: "optional Uninterruptible Power Supply (UPS) capacitors *or* battery (for emergency shutdown operations)." Bonella, [0029] (emphasis added); Dec., ¶ 198. Capacitors are not a "*battery*," so when Bonella's capacitors power the memory module for emergency shutdown operations ("*in the second mode of operation*"), the memory module "*is not powered by a battery*." Dec., ¶ 198.

Best and Bonella are both analogous art to the '833 Patent because each is from the field of memory systems. Ex. 1001, 3:60-63; Best, [0001]; Bonella, [0002]; Dec., ¶ 175.

As of the priority date of the '833 Patent, it would have been obvious to a POSITA to include Bonella's capacitors as non-battery power sources and associated powering techniques in Best's hybrid memory devices because to do so would have been merely an arrangement of old elements (Best's hybrid memory device system and Bonella's power capacitors and associated powering techniques), each performing the same function it had been known to perform (Bonella's power capacitors and associated powering techniques being used to power Best's hybrid memory device system), in a way that yields no more than a POSITA would expect from such an arrangement (Bonella's power capacitors powering Best's hybrid memory device system when operating under emergency/power-loss/power-down conditions). Best, [0025]-[0026]; Bonella, [0029]-[0031], [0033], [0101]; Dec., ¶

199. For example, as combined, Best's system would use Bonella's power techniques/capacitors to power Best's hybrid memory device system when Best's hybrid memory device system is also operating in a state similar to Bonella's "emergency shutdown operations," such as Best's operation in response to "power-loss"/"power-down" events. *Id.* As shown here, such a modification would have been obvious.

Therefore, Bonella discloses or renders obvious claims 3 and 19, and claims 3 and 19 are unpatentable as obvious over Best, Bonella, and Mills.

5. Claims 4 and 20

Claims 4 and 20 depend on claims 1 and 15, respectively, and further recite "*wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition.*"

Best teaches that, when no write-back trigger is detected, data from the host system is initially "stored in a fast-access volatile storage die" ("*first mode of operation*"). Best, [0025]-[0026]; Dec., ¶ 202. "Some time after one or more data write operations have been performed, a write-back trigger is detected" ("*a trigger condition*"), e.g., a power-loss event write-back trigger is detected. Best, [0025]-[0026]; Dec., ¶ 202. Best discloses that in response to detection of the write-back trigger ("*in response to a trigger condition*"), "one or more internal data transfer operations are performed to transfer data … from the DRAM to … the NV memory"

("*the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition*"). Best, [0025]-[0026]. Dec., ¶ 202. Therefore, Best discloses or renders obvious claims 4 and 20, and claims 4 and 20 are unpatentable as obvious over Best, Bonella, and Mills.

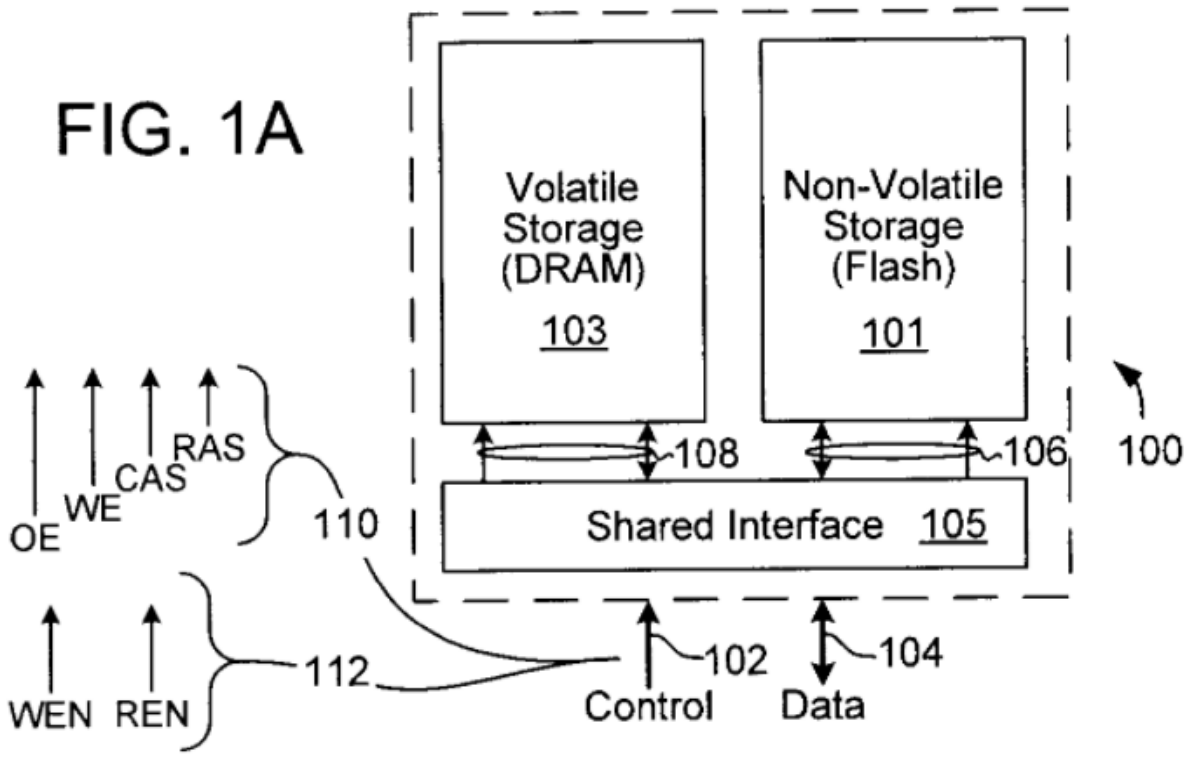
6. Claims 5 and 21

Claims 5 and 21 depend on claims 4 and 20, respectively, and further recite "*wherein the trigger condition comprises a power failure condition.*" As discussed above in §§V.C.1.b-c, Best describes that "[t]he write-back trigger itself may include … detecting a power-loss or power-down signal or event." Best, [0026]. Therefore, Best discloses claims 5 and 21, and claims 5 and 21 are unpatentable as obvious over Best, Bonella, and Mills. Dec., ¶ 204.

7. Claims 6 and 22

Claims 6 and 22 depend on claims 1 and 15, respectively, and further recite "*wherein the memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board.*" Best discloses that "the DRAM and Flash are typically implemented in separate integrated circuit devices having distinct control and data interfaces and disposed in distinct regions of an integrated circuit board." Best, [0002]. Best also states that Fig. 1A, reproduced below, "illustrates an embodiment

of a hybrid, composite memory device 100 having a non-volatile storage IC 101, volatile storage IC 103 and shared-interface IC 105."



Id., Fig. 1A, ¶13. Therefore, Best discloses claims 6 and 22, and claims 6 and 22 are unpatentable as obvious over Best, Bonella, and Mills. *See* Dec., ¶ 205.

8. Claims 7 and 23

Claims 7 and 23 depend on claims 1 and 15, respectively, and further recite "*wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation*."

Best does not explicitly disclose the foregoing features of claims 7 and 23, but it would have been obvious, in light of Mills, to include those features in the system of Best. Dec., ¶ 206.

For example, the '833 Patent describes that "the non-volatile memory subsystem 40 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation." Ex. 1001, 7:48-51. Mills teaches the same thing. Mills teaches that "[w]hen a program is to be executed, the computer system uses a technique known as shadowing to copy the code and data required to execute the program from the slow nonvolatile memory to the faster volatile memory." Mills, 3:21-36. "The shadow copy in the [volatile] main memory is then used to execute the program." *Id.* Mills also teaches that "because an unexpected power failure will cause the contents of the volatile main memory to be lost, it is common to save *intermediate* results generated during the course of execution of the program" by the host "computer system" ("*intermediate data from a host computer system computation*"). *Id.* (emphasis added); Dec., ¶ 207. Then, "[i]f any changes are made to the shadow copy during the course of the program execution," e.g., changes to the "intermediate results" saved in the volatile main memory ("*intermediate data from a host computer system computation*"), "the shadow copy [e.g., intermediate results] can be copied back [from the volatile main memory] to the slower nonvolatile memory" ("*data communicated between the*

volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation"). Mills, 3:21-36; Dec., ¶ 207.

As to the combination, as explained above in §V.C.1.c, Best and Mills are analogous art to the '833 Patent because each is from the field of memory systems. Ex. 1001, 3:60-63; Best, [0001]; Mills, 6:57-59; Dec., ¶ 208.

As of the priority date of the '833 Patent, it would have been obvious to a POSITA that Best's "transfer [of] data … from the DRAM to … the NV memory" ("*data communicated between the volatile memory subsystem and the non-volatile memory subsystem*"), e.g., during a shadow operation, would include the transfer of "intermediate results generated during the course of execution of the program" ("*intermediate data from a host computer system computation*"), such as disclosed in Mills, because to do so would have been merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement. Best, [0025]-[0026]; Mills, 3:21-36; Dec., ¶¶ 209-211. For example, as combined, Best's system would operate as usual such that when "a write-back trigger is detected," such as a power-loss event, shadowing operations are performed, e.g., "internal data transfer operations are performed to transfer data … from the DRAM to … the NV memory," where the data being transferred in Best's system includes the "intermediate results" disclosed by Mills, as described above. *Id.*

A POSITA would also have been motivated to make such a combination. Dec., ¶ 212. For example, when Best's system experiences a "power-loss" event that initiates the "performing [of] all necessary write-backs," a POSITA would have been motivated to also have Best's system write-back the "intermediate results" disclosed by Mills when "performing all necessary write-backs" to prevent the loss of all data forever, especially because prevention of data loss is a goal of both Best and Mills. Best, [0025]-[0026]; Mills, 3:21-36; Dec., ¶ 212. And a POSITA would have had a reasonable expectation that Best and Mills would successfully operate together as described because both Best and Mills disclose that the foregoing combined operations of Best and Mills are part of "shadow operation[s]." *Id.*

Therefore, Mills discloses or renders obvious claims 7 and 23, and claims 7 and 23 are unpatentable as obvious over Best, Bonella, and Mills.

9. Claims 8 and 24

Claims 8 and 24 depend on claims 1 and 15, respectively, and further recite "*wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation.*"

The '833 Patent suggests that the "non-volatile memory subsystem" acts "as a flash 'mirror' to provide backup of [data in] the volatile memory subsystem." Ex. 1001, 7:41-44.

Best's "memory shadowing" operations function the same way as the '833 Patent's "flash mirror" backup operation to provide backup of data in the volatile memory. Dec., ¶¶ 215-216. For example, Best's description of its "memory shadowing" operation teaches that "[i]nitially, data is stored in a fast-access volatile storage" and then later, in response to a write-back trigger, "write-back operations" ("*backup operation*") are performed "to transfer data … from the DRAM to … the NV memory." Best, [0024]-[0025]; Dec., ¶ 216. Best states that "[a]fter the write-back operations" ("*backup operation*") are complete there is "now-coherent data storage (i.e., same-valued data in both the volatile and non-volatile storage devices)" ("*data ... is backup data*"). Best, [0025]. Thus, the "memory shadowing" operations described by Best teach that "*backup data from a backup operation*" is "*communicated between the volatile memory subsystem and the non-volatile memory subsystem*." *Id.*, [0024]-[0025]; Dec., ¶¶ 215-216, 218-219. Therefore, Best discloses claims 8 and 24, and claims 8 and 24 are unpatentable as obvious over Best, Bonella, and Mills.

10. Claims 9 and 25

Claims 9 and 25 depend on claims 8 and 24, respectively, and further recite "*wherein the backup operation is conducted at repeating time intervals.*" As discussed above in §§V.C.1.b-c, Best's "write-back operations" ("*the backup operation*") occur in response to when a "write-back trigger" is detected. Best,

[0025]; Dec., ¶ 220. Best explains that "[t]he write-back trigger itself may include … periodically performing write-back" ("*conducted at repeating time intervals*"). Best, [0026]; Dec., ¶ 220. Therefore, Best discloses claims 9 and 25, and claims 9 and 25 are unpatentable as obvious over Best, Bonella, and Mills.

11. Claims 10 and 26

Claims 10 and 26 depend on claims 9 and 25, respectively, and further recite "*wherein the backup operation is initiated in response to a trigger event.*" As discussed above in §§V.C.1.b-c, Best's "write-back operations" ("*the backup operation*") occur "*in response*" to when a "write-back trigger" is detected. Best, [0025]; Dec., ¶ 221. Further, Best explains that the *trigger event* "include[s] any number or combination of stimuli, including detecting that the write-back table has a threshold number of valid entries; periodically performing write-back …; detecting a power-loss or power-down signal or event …; receiving an explicit command … and so forth" ("*a trigger event*" that "*initiate[s]*" the "*backup operation*"). Best, [0026]; Dec., ¶ 221. Therefore, Best discloses claims 10 and 26, and claims 10 and 26 are unpatentable as obvious over Best, Bonella, and Mills.

12. Claims 11 and 27

Claims 11 and 27 depend on claims 1 and 15, respectively, and further recite "*wherein the second mode of operation comprises a backup operation in which data*

is communicated from the volatile memory subsystem to the non-volatile memory subsystem."

As explained above in connection with claims 8 and 24 in §V.C.9, Best's "memory shadowing" write-back operations disclose or render obvious the '833 Patent's *backup operation*. Dec., ¶ 223. As explained above in §§V.C.1.b-c, V.C.2, and V.C.9, the operation of Best's system when a power-loss event write-back trigger is detected ("*the second mode of operation*") includes the performance of write-back operations ("*backup operation[s]*") in which "internal data transfer operations are performed to transfer data … from the DRAM to … the NV memory" ("*in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem*"). Best, [0025]-[0026]; Dec., ¶ 223. Therefore, Best discloses claims 11 and 27, and claims 11 and 27 are unpatentable as obvious over Best, Bonella, and Mills.

13. Claims 12 and 28

Claims 12 and 28 depend on claims 1 and 15, respectively, and further recite "*wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem.*"

As discussed above in §§V.C.1.b-c and V.C.2, Best discloses and/or renders obvious the "*second mode of operation in which data is communicated between the*

volatile memory subsystem and the non-volatile memory subsystem." Dec., ¶ 226. Best discloses additional operations within the second mode of operation, including that "a non-volatile image of the DRAM contents [] may be quickly *restored* from the Flash memory to the DRAM for rapid device boot-up and wake-up." Best, [0012] (emphasis added); Dec., ¶ 226. Specifically, Best discloses that communication between the volatile memory and the non-volatile memory ("*the second mode of operation*") includes the performance of restore operations ("*restore operation[s]*") in which data is "transferred … from the non-volatile die 101 to the volatile storage die 103 … to *restore* the state of the volatile storage die 103 to a pre-power-down or pre-sleep condition" ("*in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem*"). Best, [0021] (emphasis added); Dec., ¶ 226. Therefore, Best discloses claims 12 and 28, and claims 12 and 28 are unpatentable as obvious over Best, Bonella, and Mills.

14. Claims 13 and 29

Claims 13 and 29 depend on claims 1 and 15, respectively, and further recite "*wherein one or more of the first, second or third clock frequencies is configurable by the memory system.*"

It would have been obvious, in light of Bonella, to include the features of claims 13 and 29 in the system of Best. Dec., ¶ 229.

In particular, memory devices including configurable frequency settings were well-known in the art by the '833 Patent's priority date. *Id.*, ¶ 230. For example, Bonella explains that the memory module has power management features that are "user configured and/or system configured." Bonella, [0045]; Dec., ¶ 230. These power management features include the DRAM frequency reduction functionality. Bonella, [0049]-[0050]; Dec., ¶ 230. Specifically, Bonella explains that Power Level 4 "reduces power by limiting the DRAM performance" and is "user configurable." Bonella, [0048]. This configuration information is obtained by the memory controller, which then uses the information to carry out any necessary power reduction. *Id.*, [0045]; Dec., ¶ 230.

Bonella also teaches that the DRAM interface can correspond to the "DDR2 DRAM specification," Bonella, [0036], and the operational frequencies of DDR2 DRAM were configurable, Dec., ¶ 231; *see, e.g.*, Ex. 1017, 47 ("The user may change the external clock frequency"), 53 ("DDR2 SDRAM input clock frequency can be changed"); *see, e.g.*, *id.*, 75 (listing a minimum and maximum clock cycle time (tCK) (i.e., the inverse of the input clock frequency) for DDR2-400). Bonella thus teaches to a POSITA that at least the primary operating frequency of the DRAM (i.e., the "*first clock frequency*") "*is configurable by the memory system*" based on the user configuration. Dec., ¶ 231.

Best and Bonella are both analogous art to the '833 Patent because each is from the field of memory systems. Ex. 1001, 3:60-63; Best, [0001]; Bonella, [0002]; Dec., ¶ 232.

As of the priority date of the '833 Patent, and at least in light of Bonella, it would have been obvious to a POSITA to make "*one or more of the first, second or third clock frequencies*" associated with Best's DRAM or Flash memory "*configurable by the memory system*" at the direction of a user. Dec., ¶ 233. For example, as explained above, DDR2 SDRAM allowed for configurable input clock frequencies (either the "*first*" or "*third clock frequencies*"), and Bonella suggests that the system's power management features are "user configured and/or system configured." *See id.*, ¶¶ 230-233. Bonella also suggests adjusting the operational frequency of DRAM to reduce power consumption. Bonella, [0049]-[0050]; Dec., ¶ 233. Even Flash memory clocks were known to be configurable. Dec., ¶ 233; *see, e.g.*, Ex. 1019, 25 (Table 8) (showing configurable frequencies).

A POSITA would have thus been motivated to make "*one or more of the first, second or third clock frequencies*" associated with Best's DRAM or Flash memory "*configurable by the memory system*" at the direction of the user, based at least on Bonella, to obtain the benefit of configurability and power savings. Dec., ¶ 234. To allow for Bonella's configurability in the system of Best would also have been merely an arrangement of old elements (Best's hybrid memory device system and

Bonella's power and DRAM operational frequency configuration techniques), each performing the same function it had been known to perform (Bonella's configuration techniques being used to configure at least the clock frequency of the DRAM in Best's system and Best's DRAM operating in the same manner as before), in a way that yields no more than a POSITA would expect from such an arrangement (Best's DRAM operating as usual with the addition of the clock frequency being configurable based on Bonella's configuration techniques to selectively reduce power based on user need). *Id.* As shown here, such a combination would have been obvious.

Therefore, Bonella discloses or renders obvious claims 13 and 29, and claims 13 and 29 are unpatentable as obvious over Best, Bonella, and Mills.

15. Claims 14 and 30

Claims 14 and 30 depend on claims 1 and 15, respectively, and further recite "*wherein one or more of the first, second or third clock frequencies is configurable by a user*."

It would have been obvious, in light of Bonella, to include the features of claims 14 and 30 in the system of Best. Dec., ¶ 237.

In particular, memory devices including user-configurable frequency settings were well-known in the art by the '833 Patent's priority date. *Id.*, ¶ 238. For example, as explained above in §V.C.14, Bonella explains that "*one or more of the first,*

second or third clock frequencies is configurable by the memory system" at the direction of the user. *See id.*, ¶ 238; *see, e.g.*, Bonella, [0045] ("user configured and/or system configured"), ¶48 (explaining that Power Level 4, which "reduces power by limiting the DRAM performance," is "user configurable."); Ex. 1017, 47 ("The user may change the external clock frequency ….). Also, as explained above in §V.C.14, those features are also obvious. *See* Dec., ¶ 238. Therefore, Bonella also discloses and/or renders obvious that "*one or more of the first, second or third clock frequencies is configurable by a user*." Bonella, [0045], [0048]-[0050]; Dec., ¶ 238.

Best and Bonella are both analogous art to the '833 Patent because each is from the field of memory systems. Ex. 1001, 3:60-63; Best, [0001]; Bonella, [0002]; Dec., ¶ 239.

For the same reasons that it would have been obvious to a POSITA, at least in light of Bonella, to make "*one or more of the first, second or third clock frequencies*" associated with Best's DRAM or Flash memory "*configurable by the memory system*" at the direction of a user, as explained above in §V.C.14, it would have been obvious to a POSITA to make "*one or more of the first, second or third clock frequencies*" associated with Best's DRAM or Flash memory "*configurable by a user*." Dec., ¶ 240. In addition, a POSITA would have been motivated, at least in light of Bonella, to make "*one or more of the first, second or third clock frequencies*" associated with Best's DRAM or Flash memory "*configurable by a*

user," for at least the same motivation reasons explained above in §V.C.14. Dec., ¶ 240. As shown, such a combination would have been obvious.

Therefore, Bonella discloses or renders obvious claims 14 and 30, and claims 14 and 30 are unpatentable as obvious over Best, Bonella, and Mills.

D. No Secondary Considerations Exist

No secondary indicia of non-obviousness exist. Petitioners reserve their right to respond to any assertion of secondary indicia of non-obviousness advanced by Netlist.

VI. The Parallel Litigation Does Not Warrant Denying Institution

When considering a parallel proceeding, the PTAB "balance[s] considerations such as system efficiency, fairness, and patent quality" using the six factors set forth by the Board in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5 (PTAB Mar. 20, 2020) (precedential). These factors "overlap," and a "holistic view" should be taken. *Id.*, p. 6.

The fourth factor (overlap) strongly favors institution. Petitioners have stipulated to not pursue invalidity based on Ground 2—or even the Ground 2 references—if the Board institutes trial in this proceeding. Ex. 1014. Petitioners modeled this stipulation on the stipulation that the Board found to "mitigate any concerns" in *VMware, Inc. v. Intellectual Ventures I LLC*, IPR2020-00470, Paper 13 at 20 (PTAB August 18, 2020). This fourth factor favors institution

here even more so than in *Apple, Inc. v. SEVEN Networks, LLC*, IPR2020-00156, Paper 10 (PTAB June 15, 2020). There, the petitioner provided no stipulation. *Id.* pp. 16-19. Nevertheless, the fourth factor "strongly favored" petitioner. *Id*. Furthermore, this Petition challenges claims 1 and 3-14, which are not at issue in the parallel litigation. The claims-at-issue in both proceedings do not overlap, thus another reason that the fourth factor favors institution.

The third factor (investment in parallel proceeding) also favors institution. The district court has not yet issued any substantive opinions regarding the scope or validity of the Challenged Claims, and given Petitioners' stipulations, the Court is unlikely to invest any resources on Ground 2 raised in this Petition, either before or after the scheduled institution date. Furthermore, the parallel proceeding is in an early stage, fact discovery has not yet opened, and no trial date has been set. Only initial contentions have been exchanged. Ex. 1020.

Regarding the sixth factor (merits, other circumstances), the merits strongly weigh in favor of instituting trial as shown through the strength of the grounds in this Petition. Other circumstances also favor institution. Like in *Apple v. SEVEN*, the parallel litigation is complex, involving substantial litigation history and IPR history regarding the '833 Patent and the family of patents associated with the '833 Patent, 15 asserted claims, and many accused products, and the district court requires reduction of claims and prior art references pre-trial. *SEVEN*, 21-22; Ex. 1021, 10

(weighing claim reductions). An IPR trial, in contrast, allows a focus on resolving all challenged claims in a single patent, thus "enhanc[ing] the integrity of the patent system." *SEVEN*, 22.

Fintiv factors 1 (stay) and 2 (proximity of trial dates) favor institution. Petitioners do not know if the district court will stay the case if trial is instituted, and the Court has not yet set the trial date. The scheduling order in the related litigation lists dates only up to the tentative *Markman* Hearing date. Ex. 1020; *compare Micron Tech., Inc. v. Godo Kaisha IP Bridge 1*, IPR2020-01007, Paper 15 at 10-13 (PTAB December 7, 2020) ("[The] proximity factor in *Fintiv*, on its face, asks us to evaluate our discretion in light of trial dates that have been set in parallel litigations, not to speculate as to trial dates that are still to-be-determined."). Without a scheduled trial date, the Board should consider these two factors "weigh[ing] strongly against exercising [PTAB's] discretion to deny institution." *See Shure Inc. v. Clearone, Inc.*, PGR2020-00079, Paper 14 at 15–16, (February 16, 2021) ("[U]nlike in the *NHK* and *Fintiv* cases, there is no trial date set in the Illinois case. Thus, this factor weighs strongly against exercising our discretion to deny the Petition."); *Sand Revolution II, LLC v. Cont'l Intermodal Grp–Trucking LLC*, IPR2019-01393, Paper 24 at 8-10 (June 16, 2020) (informative).

For these reasons, the Board should not exercise its discretion to deny institution of this Petition.

VII. Past IPRs Do Not Warrant Denying Institution

When considering whether to exercise its discretion under 35 U.S.C § 314(a), the PTAB may consider seven factors set forth by the Board in *General Plastic Industrial Co. v. Canon Kabushiki Kaisha.*, IPR2016-01357, Paper 19 (PTAB Sept. 6, 2017) (precedential). As explained below, all factors favor institution or are neutral.

Factor 1 strongly favors institution because all prior IPR challenges involved a different petitioner(s) than Petitioners here, and this Petition involves a different prior art combination (Best, Bonella, and Mills) that was not at issue in any of the previous IPR challenges against the '833 Patent.

Factor 5 also favors institution because Petitioners were not involved in any of the previous IPR petitions against the '833 Patent, nor had Petitioners received notice of the '833 Patent until recently in connection with the parallel district court litigation.

Factor 6 also favors institution. As shown in Ground 1 above (§V.B), the Board has already considered and decided the issues raised in this Petition with respect to the challenged independent claims, so review of the independent claims is simplified and streamlined in this case under the doctrine of collateral estoppel. However, the Board has not previously spent any resources considering the issues

raised in this Petition with respect to the challenged dependent claims because those are new arguments, further pushing factor 6 in favor of institution.

The remaining factors 2 through 4 and 7 are neutral because Netlist sued Petitioners almost three years after the Board issued its Final Written Decision in the latest-decided IPR for a patent related to the '833 Patent, namely the '692 IPR. *See* Ex. 1022. So any prejudice arose from Netlist's delay in filing suit—not Petitioners. Factor 7 is neutral because this Petition would not seem to affect the Board's ability to timely issue a final determination. Accordingly, no remaining factor weighs in favor of denying institution.

For these reasons, the Board should not exercise its discretion to deny institution of this Petition.

VIII. Mandatory Notices

A. Real Parties-in-Interest

Petitioners are the only entities funding and controlling this Petition and are therefore the named real parties-in-interest. No other entity is funding, controlling, or otherwise has an opportunity to control or direct this Petition or Petitioners' participation in any resulting IPR.

B. Related Proceedings

Netlist asserted the '833 Patent against Petitioners in the Western District of Texas, Case No. 6:21-cv-00430. As described above in §III.D, the '833 Patent was previously at issue in IPR2014-00994, IPR2014-01370, and IPR2017-00649.

Additionally, a nearly identical claim to the '833 Patent's claim 15 was invalidated as obvious in IPR2017-00692. For those IPRs, the petitioners were SanDisk Corporation, SMART Modular Technologies, and SK hynix.

C. Lead and Backup Counsel

Petitioners' lead and backup counsel are:

Lead Counsel for Petitioner	Backup Counsel for Petitioner
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D. Electronic Service

Petitioners consent to electronic service at:

Winston-IPR-NetList@winston.com.

IX. Fees

The required fee is being paid electronically through PTAB E2E.

X. Conclusion

Petitioners respectfully request that the Board institute IPR and enter a final written decision finding the Challenged Claims unpatentable.

Dated: January 14, 2022

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

This Petition complies with the word count limits set forth in 37 C.F.R. § 42.24(a)(1)(i), because this Petition contains 13,949 words, excluding the parts of the Petition exempted by 37 C.F.R. § 42.24(a)(1), determined using the word count provided by Microsoft Word, which was used to prepare this Petition.

Dated: January 14, 2022

Respectfully submitted,

/ *Juan C. Yaquian* /

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CERTIFICATE OF SERVICE

Under 37 C.F.R. §§ 42.6(e) and 42.105(a), this is to certify that on January 14, 2022, I caused to be served a true and correct copy of the foregoing "**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,301,833**" and Exhibits 1001-1022 by Federal Express on the Patent Owner at the correspondence address of record for U.S. Patent No. 8,301,833:

Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 2006-1152

A courtesy copy of this Petition and supporting material was also served on litigation counsel for Patent Owner via email:

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